The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JOSEPH C. SHER and DANIEL R. LOUGHMILLER

Appeal No. 2005-0826
Application No. 09/989,563

HEARD: May 24, 2006

Before HAIRSTON, BLANKENSHIP, and SAADAT, Administrative Patent Judges.

BLANKENSHIP, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-16 and 25, which are all the claims remaining in the application.

We affirm, and enter new grounds of rejection in accordance with 37 CFR § 41.50(b).

BACKGROUND

The invention relates to differential voltage regulators used in semiconductor devices. Representative claim 1 is reproduced below.

> 1. A voltage control circuit which provides a test supply voltage during manufacturing and testing of a semiconductor device and an operational supply voltage after certification of the semiconductor device, the operational supply voltage being lower than the test supply voltage, the voltage control circuit comprising:
>
> a clamp circuit having a plurality of voltage regulation devices, the voltage regulation devices controlling a clamping threshold of the clamp circuit;
>
> a voltage regulator electrically coupled to the clamp circuit which generates a first control signal responsive to the clamping threshold of the clamp circuit;
>
> a charge pump which receives the control signal from the voltage regulator, the charge pump generating the test supply voltage; and
>
> at least one bypass device connected to at least one of the plurality of voltage regulation devices, wherein the at least one bypass device is activated following the certification of the semiconductor device to bypass the at least one of the plurality of voltage regulation devices from the clamp circuit to lower the clamping threshold of the clamp circuit, the voltage regulator generating a second control signal responsive to the lowered clamping threshold of the clamp circuit to cause the charge pump to generate the operational supply voltage.

The examiner relies on the following references:

Furumochi	5,473,277	Dec. 5, 1995
Javanifard et al. (Javanifard)	5,483,486	Jan. 9, 1996

Claims 1-16 and 25 stand rejected under 35 U.S.C. § 103 as being unpatentable over Javanifard and Furumochi.

We refer to the Final Rejection (mailed May 31, 2002) and the Examiner's Answer (mailed Mar. 31, 2003) for a statement of the examiner's position and to the Brief (filed Jan. 10, 2003) and the Reply Brief (filed Jun. 5, 2003) for appellants' position with respect to the claims which stand rejected.

OPINION

Rejection over the prior art

Consistent with appellants' Brief and the rules effective at the time of its filing, we select claims 1 and 10 as representative for the purposes of this appeal. See 37 CFR § 1.192(c)(7) (2002).

The examiner finds that Javanifard shows in Figure 14 a voltage control circuit within the meaning of instant claim 1, except that voltage reference 316 does not contain a plurality of voltage regulation devices and at least one bypass device connected to at least one of the plurality of voltage regulation devices. The examiner turns to Furumochi (Fig. 5) and its teaching of a plurality of voltage regulation devices (T1-T4) with at least one bypass device (SW0(TN4)) connected to at least one of the plurality of voltage regulation devices. The examiner finds that the prior art suggested combination of the references for the purpose of providing an adjustable (i.e., finely adjustable) reference voltage in the device of Javanifard. The examiner concludes that the subject matter as a whole of instant claim 1 would have been prima facie obvious to the artisan. (Answer at 3-4.)

Appellants' main contention in the briefs is that neither reference discloses or suggests a "clamp circuit" as claimed. In the examiner's opinion, as set out at pages 11 and 12 of the Answer, the diodes described by Furumochi operate as a "clamp circuit" within the meaning of the claim.

Instant claim 1 recites, "a clamp circuit having a plurality of voltage regulation devices, the voltage regulation devices controlling a clamping threshold of the clamp circuit. . . ." The claim further recites a voltage regulator electrically coupled to the clamp circuit which generates a first control signal "responsive to the clamping threshold of the clamp circuit. . . ."

Appellants argue and rely on language that does not appear in claim 1, seemingly on the basis that the artisan would recognize that a "clamp circuit" and a "clamping threshold" would require more than the features expressed in the claim. However, appellants have provided no extrinsic evidence, such as a section of a relevant text in the art, in support of the allegations. Arguments of counsel are not evidence. See, e.g., Meitzner v. Mindick, 549 F.2d 775, 782, 193 USPQ 17, 22 (CCPA 1977); In re Pearson, 494 F.2d 1399, 1405, 181 USPQ 641, 646 (CCPA 1974).

The instant specification describes a "clamp circuit" 210 (Fig. 3A). According to paragraphs 39 and 40 of the written description, the clamp circuit operates to limit the voltage at node 319. As voltage V_{CCR} increases, the diodes 305, 307, 309, 311, and 313 slowly turn on to "clamp" the maximum voltage at node 319 to the total voltage across the five diodes. This results in a fixed voltage at node 319. The "clamp circuit"

thus appears to consist of resistor 301 connected with diodes 305, 307, 309, 311, and 313. Two capacitors (315, 317) are also connected to node 319, but are not said to contribute to the clamping function. The capacitors act as buffers to prevent rapid change of the voltage at node 319. Figure 4A depicts a clamp circuit with a fuse control (bypass device) 400. (Spec. ¶ 41.)

Furumochi at Figure 5 depicts resistance RL connected with diode-configured transistors (i.e., diodes) T1 through T4. Furumochi's invention is an improvement over the prior art circuit shown in Figure 1 and further described at column 5, lines 18 through 54. In the prior art, selected output voltages were dependent of the thresholds VTH of selected diode-configured transistors. Due to variability in manufacturing of the transistors serving as diodes, only a "rough" adjustment of output voltage was possible. We note that the prior art with respect to Furumochi also contained bypass devices TS1 through TS3, for selecting diodes and thus determining the output voltage of the circuit.

Furumochi uses a "bias variable means" 11 (Fig. 3) to selectively bias the back-gate of transistors, effecting control of the transistor threshold voltages. Control of the voltage output of the bias variable means, in turn, is effected by a ROM fuse circuit 14 that may be programmed for generating particular external control signals. Col. 5, l. 55 - col. 7, l. 10.

In Furumochi's Figure 5, the switching element SW0 and selection switching circuit SW1-SW3 constitute an illustrative example of a bias variable means. The switching element SW0 is an example of the switching element 11A, shown in Figure 3.

Switching element SW0 is composed of a field effect transistor with its gate connected to the ROM fuse circuit 14. Col. 7, ll. 39-50. An equivalent circuit is depicted in Figure 6. Col. 5, ll. 30-35.

Programming of the ROM fuse circuit 14 is described at column 9, line 12 et seq. of the reference. Various examples are provided in Figure 7A through Figure 8D, showing equivalent circuits, responsive to how the ROM fuse circuit may be programmed by melting and disconnecting particular fuse elements. Figure 8A represents the bypassing of diode T4 by programming SW0 as "ON."

Different output voltages for the circuit of Figure 5 are thus effected by controlling the total threshold voltages of the diodes, the sum of which sets the circuit's constant output voltage V_{DD}. In appellants' "clamp circuit" as described in the specification, the threshold voltages of the diodes are not controlled individually. However, the relevant circuit in Furumochi appears to operate on the same principle as appellants' "clamp circuit." The instant clamp circuit operates to limit the voltage at (output) node 319 (instant Fig. 3A) corresponding to the summation of the threshold voltages of the diodes. In Furumochi's circuit of Figure 5, the output voltage V_{DD} appears to be determined by the sum of the threshold voltages of the diodes.

The record thus supports the examiner's finding that Furumochi describes a clamp circuit having a clamping threshold within the meaning of instant claim 1. Appellants may hold that what appellants consider to be a "clamp circuit" might operate differently from the circuit described by Furumochi when placed in some other

environment. However, as we have noted, appellants have not provided evidence in support of such a view. On this record, we find ample support for the examiner's position, which is not demonstrated to be erroneous by appellants' arguments.

Appellants are correct in the assessment of Furumochi to the extent of the statement bridging pages 7 and 8 of the Brief: "When in an 'ON' state, the switching element bypasses a transistor T4 and causes the output voltage of the voltage generator circuit [to] be at a lower level." Appellants allege that "[t]his switching element, however, cannot be activated to bypass a voltage regulation device in order to lower a clamping threshold." (Brief at 7.) Appellants' argument in support of the allegation, according to the paragraph bridging pages 7 and 8 of the Brief, is that the switching element disclosed by Furumochi cannot switch from the "OFF" to the "ON" state because to be in the "OFF" state, fuse elements of the ROM fuse circuit are melted and disconnected. In support of this argument, appellants direct our attention to column 9, lines 22 through 33 of Furumochi. Column 9, lines 22 through 37 of Furumochi discusses melting and disconnecting fuses of the ROM fuse circuit for generating external control signals; in particular, melting and disconnecting of fuses with respect to SW1, SW2, and SW3 (Fig. 6). The section does not describe melting or disconnecting fuses to effect the "OFF" state of SW0. Moreover, the rejection is based on what the artisan would have found obvious, rather than identity of disclosure. Even if the switch (SW0) of Furumochi were to operate in the way not shown by appellants, the question would be raised as to why melting fuses to effect either of an "ON"

(bypass) and "OFF" (no bypass) state would not have been considered equally obvious to one skilled in the relevant art.

We are not persuaded by appellants' allegations (Brief at 8-9) that the references "teach away" from the invention, or that a reference would be rendered unsatisfactory for its intended purpose. Appellants' allegations are based on the position that neither reference teaches a "clamp circuit." Appellants' position is untenable, in view of the evidence of this record, which includes the teachings of Furumochi.

Appellants further submit, in the Reply Brief, that Javanifard does not refer to the output voltage (Fig. 14) as a test voltage, and does not disclose or suggest any variation in the output voltage for test purposes.

Appellants seem to appreciate that instant claim 1 is directed to a voltage control circuit (i.e., an apparatus), rather than a process. How the circuit is intended to be used does not change the characteristics of the circuit itself. For example, an output voltage of 5 Volts is 5 Volts regardless of how one may refer to the output. Thus, we agree with appellants that Javanifard does not refer to the output voltage as a test voltage. We disagree to any extent that appellants may hold that claiming the charge pump to generate a "test" supply voltage might distinguish over the applied prior art.

The combination as proposed by the examiner provides a first voltage output (e.g., from charge pump 320 of Javanifard) and a second, lower voltage output (from the charge pump) following activation of a bypass device, according to the teachings of Furumochi. We have considered all of appellants' arguments in response to the

rejection for prima facie obviousness with respect to instant claim 1, but the arguments do not persuade us that the claim has been rejected in error.

Appellants submit that claims 10 through 14 are separately patentable because the "means plus functions limitations" must be examined in accordance with the guidelines set forth in the Manual of Patent Examining Procedure (MPEP). Appellants do not tell us in what way the examination has been not in accordance with the MPEP guidelines, nor in what way the allegation might be considered an argument in support of separate patentability of the claims.

Aside from repeating language from claim 10, which is not an argument for separate patentability (see 37 CFR § 1.192(c)(7) (2002); see also 37 CFR § 41.37(c)(1)(vii) (2005)), appellants submit in the Brief that neither Javanifard nor Furumochi discloses or suggests a voltage control circuit having a clamp circuit. For the reasons set forth in our discussion of the rejection of claim 1, we do not find the allegation persuasive.

In the Reply Brief (at 5), appellants submit that the proposed combination is "not structurally or functionally equivalent to the disclosed combination of elements" as claimed in claim 10. We have noted supra (in the discussion of claim 1), however, the similarities in appellants' circuit and the applied prior art. Appellants do not point out any disclosed structure that may differ from the applied art. Appellants do allege that the "means for generating a first control signal" includes circuitry that receives the test supply voltage as feedback for controlling the test supply voltage.

First, appellants have not shown that the unexpressed limitation is required by instant claim 10. Section 112, paragraph 6 does not permit incorporation of structure from the written description beyond that necessary to perform the claimed function. Structural features that do not actually perform the recited function do not constitute corresponding structure and thus do not serve as claim limitations. Asyst Technologies, Inc. v. Empak, Inc., 268 F.3d 1364, 1369-70, 60 USPQ2d 1567, 1571 (Fed. Cir. 2001) (citations omitted). Second, even if claim 10 were to require such a limitation, Javanifard describes (Fig. 14; col. 19, ll. 9-28) feedback from the output voltage (to divider circuit 317) for controlling the output voltage, and thus includes circuitry that receives the "test supply voltage" as feedback for controlling the "test supply voltage" within the meaning of the claim.

We therefore sustain the rejection of claims 1 and 10 under 35 U.S.C. § 103 as being unpatentable over Javanifard and Furumochi, and of claims 2-9, 11-16, and 25 that fall with claim 1 or claim 10.

New grounds of rejection

We enter the following new grounds of rejection against the claims in accordance with 37 CFR § 41.50(b): Claims 15 and 16 are rejected under 35 U.S.C. § 112, first paragraph, as the specification lacks adequate written description and enablement for claimed subject matter.

> The "written description" clause of section 112 has been construed to mandate that the specification satisfy two closely related requirements. First, it must describe the manner and process of making and using the invention so as to enable a person of skill in the art to make and use the full scope of the invention without undue experimentation. Second, it must describe the invention sufficiently to convey to a person of skill in the art that the patentee had possession of the claimed invention at the time of the application, i.e., that the patentee invented what is claimed. Those two requirements usually rise and fall together. That is, a recitation of how to make and use the invention across the full breadth of the claim is ordinarily sufficient to demonstrate that the inventor possesses the full scope of the invention, and vice versa.

LizardTech, Inc. v. Earth Resource Mapping, Inc., 424 F.3d 1336, 1344-45, 76 USPQ2d 1724, 1731-32 (Fed. Cir. 2005) (citations omitted).

Instant claim 16 depends from independent claim 15. Claim 15 is similar to instant claim 1. Claim 15, however, recites that the at least one bypass device is "reversibly activated to reversibly bypass the at least one of the plurality of voltage regulation devices from the clamp circuit, thereby modifying the clamping threshold of the clamp circuit."

The specification, at page 13, describes bypass device 400 (Fig. 4), whereby either or both of fuses 415 and 420 may be blown, effectively removing diodes 311 and 313 from the circuit. We do not find description of any kind of "reversible" bypassing. When questioned on the point at the oral hearing, appellants' representative declined to point out written description support for the feature, contending that the feature is not present in the claims that remain in the application. Instant claim 15, however, remains and contains the feature.

On this record, we conclude there is no adequate written description for the subject matter of claims 15 and 16, and further that the claims contain subject matter that was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

CONCLUSION

The rejection of claims 1-16 and 25 under 35 U.S.C. § 103 is affirmed.

New rejections of claims 15 and 16 under 35 U.S.C. § 112, first paragraph, for failure to comply with the written description requirement and failure to comply with the enablement requirement, are set forth herein.

This decision contains a new ground of rejection pursuant to 37 CFR § 41.50(b) (2005). 37 CFR § 41.50(b) provides "[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review."

37 CFR § 41.50(b) also provides that the appellant, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:

> (1) *Reopen prosecution.* Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner. . . .

(2) *Request rehearing*. Request that the proceeding be reheard under § 41.52 by the Board upon the same record. . . .

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a). See 37 CFR § 1.136(a)(1)(iv).

AFFIRMED -- 37 CFR § 41.50(b)

KENNETH W. HAIRSTON
Administrative Patent Judge

HOWARD B. BLANKENSHIP
Administrative Patent Judge

MAHSHID D. SAADAT
Administrative Patent Judge

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